FDTD Analysis of High Frequency Electronic Interconnection Effects

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Abstract—**A full-wave analysis of coupled high-frequency interconnect discontinuities is presented using the finite-difference time-domain (FDTD) method. The electromagnetic effects of two via holes on microstrip lines in close proximity to one another are examined and equivalent circuits are presented. The effects of two adjacent lines with bond wires, used, for example, to connect a die to the leadframe of an integrated circuit (IC) package are also analyzed. Frequency domain results are presented by using the discrete Fourier transform of the time-domain results. Guidelines regarding the effective use of the FDTD code including the use *a priori* calculated electric field distribution in the excitation plane, and the use of a weighted $\epsilon_{r,\text{eff}}$ to minimize reflections at the absorbing boundaries are described. The obtained FDTD results and the developed equivalent circuit models show the importance of radiation effects at frequencies beyond 20-30 GHz, the possibilities of reducing the inductive effect of bond wires by using two parallel bond wires instead of one, and the importance of including mutual inductance elements in the equivalent circuit model to account for the crosstalk between parallel vias across a ground plane.**

I. Introduction

ELECTRONIC packaging and interconnects for high performance devices, such as computers and RF/microwave devices, is an area that recently has hit the forefront of electronic design. For many applications, packages are used only for structural support and have no influence on the electronics of the device. For many other applications, however, the packages have a direct effect on the electrical performance of the enclosed circuitry. High performance computers and radio/microwave frequency integrated circuits (RF/MIC) are examples of electrical devices where packaging effects can be quite serious. At microwave frequencies interconnect dimensions are on the order of a wavelength and considerable interactions between the circuitry and the surrounding package can occur. Parameters such as cross talk (coupling), skin depth, delays, and dispersion have therefore become critically important in effective design of electronic packages. At present, it may even be said that packaging effects have become the bottleneck to high speed/high bandwidth electronics. While technology advances in areas such as semiconductors and VLSI design have chip devices operating with clock speeds beyond 10 GHz, package effects, and interconnect delays combined together can hinder the effective use of these high bandwidths. Not only do the packages have to be designed such that they can handle the high frequencies and bandwidths of operation, but the package effects on the circuits must be taken into account in order to correctly determine the operation of a circuit, especially as electronics are miniaturized. On top of that, in most cases, optimum thermal, mechanical, and electrical performance issues compete against one another and the final design is a compromise between them.

Recently, many contributions have been made in the full-wave analysis of package and interconnect discontinuities, as is shown by the recent IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES issue that was devoted to the subject [1]. Most of these contributions presented analysis of one aspect of packaging, but very few account for multiple interacting structures of a complete package or electronic system. Most printed circuit boards (PCB) use multiple-via-through holes to mount IC's such as dual-inline-packages (DIP's) or pin grid arrays (PGA's) as well as route signal lines. A typical high density pin grid array can have more than 500 pins mounted with a typical 100 mil pitch. Electromagnetic interactions between all the pins and vias can cause serious signal degradation at high frequencies and must be taken into account in the initial design phase of circuit. Recently, Picket-May *et al.* showed qualitative results for a complete 3-D connector module which included many vias [2], but in-depth quantitative results were not presented for the multilayeredd board. For IC packaging, most IC's utilize bond wires to connect the leadframe pins to the die. The bond wires are typically 1 mil (25 μm) ribbon wires and add a significant amount of inductance to the leadframe pins, thus limiting the high-frequency performance of the device. Although the inductance of a bond wire [3] and a single via hole [4] can be estimated, higher order effects such as mutual inductances, increased coupling from one microstrip line to another due to the effects of bond wires and vias or increased radiation can not be determined exactly. In this paper, we use the FDTD method to analyze two important interconnect geometries, the via and the bond wire, and give high-frequency equivalent circuit models for these structures.

II. The FDTD Algorithm

The FDTD method is a popular three-dimensional (3-D) full-wave numerical algorithm which has been used to model various electromagnetic phenomena and interactions [5], [6]. In particular, planar-type circuits have recently been analyzed [1], [7], and [8] and even more recently, the FDTD algorithm has been extended to incorporate various passive and active loads for planar type geometries [2], [9], and [10]. Various interconnection structures have also been analyzed [1]. The

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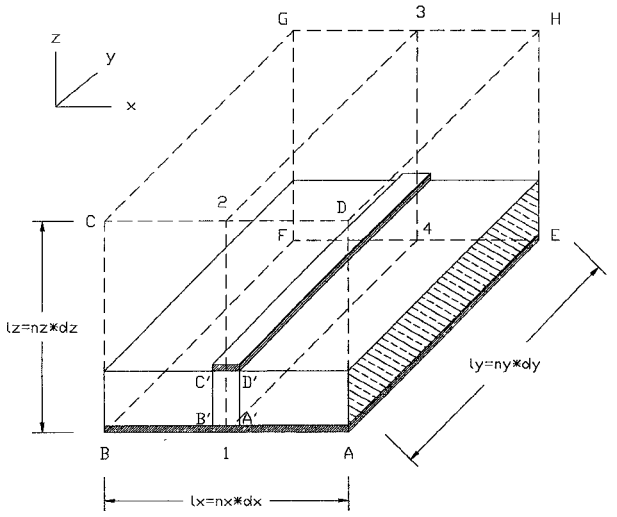


Fig. 1. Typical planar geometry modeled showing the FDTD lattice. Plane ABCD is the source plane, and plane 1234 is the symmetry plane.

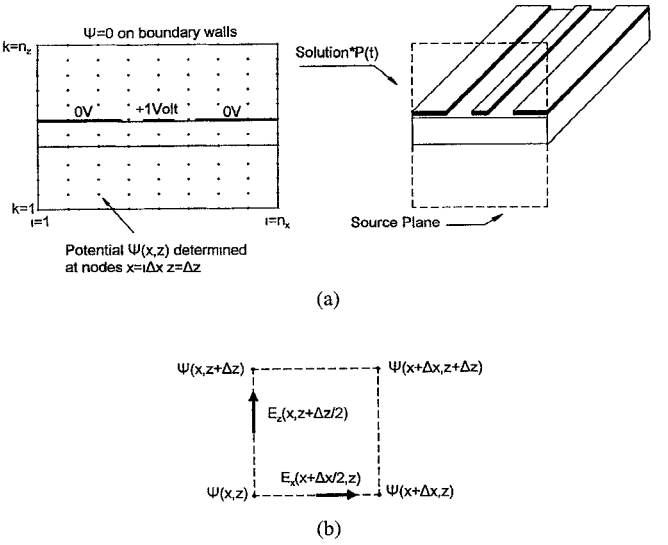


Fig. 2. Schematic showing 2-D quasi-TEM solution for the excitation source. (a) Quasi-solution is multiplied by a time varying function and added into the FDTD lattice. (b) Placement of the nodes for calculation of the static potential and the relationship to the electric field position in the Yee-cell.

FDTD method is again used in this paper to characterize two particular interconnection structures, the via and the bond wire.

The main FDTD algorithm is discussed in numerous articles and will not be discussed in detail here [5], [6], and [11]. Fig. 1 shows a schematic diagram of a typical microstrip line model using FDTD. The excitation plane is located at plane ABCD and absorbing boundary conditions (ABC) are placed at all walls of the lattice. A soft source is used, where the absorbing boundaries at plane ABCD are turned off while the source is on and the ABC is then turned on before any electromagnetic energy is reflected back toward the excitation plane. For structures which possess symmetry in the x direction, a magnetic wall is used instead of the ABC and placed at the plane 1234 which reduces computer memory and run times in half. For this research, the metallization layers of the substrate are assumed infinitely thin and perfectly conducting.

A. Excitation Source

For many uniform guiding structures, the electromagnetic field distribution is known and can therefore be used to excite the fields in the FDTD lattice. For many others, in particular, most planar circuits, the exact electromagnetic field distribution is not known and therefore cannot be used as an excitation source in the FDTD grid. For microstrip circuits, what is generally done is to assume a uniform vertical electric field between the ground plane and the microstrip line. Although for points near the center of the microstrip line this may be true, it is generally expected that this assumption is not accurate for points near the edges of the conductors. The assumed approximate source is then allowed to propagate until the correct electromagnetic field distribution is obtained, typically a few to tens of cells in the lattice. The source can be made to converge much faster by utilizing a spacial distribution which more closely resembles the actual field distribution [12], [15]. In general, the excitation source is given by

$$\overline{E}_s = E_x(x, y, z, t)\hat{x} + E_y(x, y, z, t)\hat{y} + E_z(x, y, z, t)\hat{z}. \tag{1}$$

For a structure that is uniform along the direction of propagation, e.g., the y direction, (1) can be written as

$$\overline{E}_s = (E_x(x, z)\hat{x} + E_y(x, z)\hat{y} + E_z(x, z)\hat{z})P(t) \tag{2}$$

where $P(t)$ is a time varying waveform such as a sinewave or a Gaussian pulse. For the commonly used uniform vertical electric field source in (2), the following assumptions are often made: $E_x(x, z) = E_y(x, z) = 0$ and $E_z(x, y) =$ constant under the microstrip (plane A'B'C'D'). In order to improve convergence in our FDTD code, a quasi-TEM field distribution ($E_y(x, z) = 0$) is calculated using the 2-D finite-difference (FD) Gauss–Seidel method utilizing overrelaxation [13], [14].

The 2-D FD method iteratively solves for the electrostatic potential, $\psi(x, z)$ in a region. Fig. 2(a) shows a 2-D schematic of a typical coplanar waveguide geometry which is to be solved by the FD method. By placing a voltage potential on the source conductor, the electrostatic potential distribution $\psi(x, z)$ can be calculated throughout the lattice region. The lattice boundaries are assumed to be at zero volts and, hence, are placed sufficiently far from any source conductors. The electrostatic potential is found at points which coincide with the vertices of the Yee cells in the FDTD grid. Fig. 2(b) shows the spatial relationship inside the Yee-cell for the tangential electric fields (E_x and E_z) and the calculated potentials, $\psi(x, z)$. Once the electrostatic potential is calculated, the 3-D transverse electric field components in (2) at the lattice cell $(i, 1, k)$ in the FDTD grid are calculated, using cell indices, as

$$E_z(i, 1, k) = \frac{\psi(i, k+1) - \psi(i, k)}{\Delta z} \tag{3}$$

$$E_x(i, 1, k) = \frac{\psi(i+1, k) - \psi(i, k)}{\Delta x} \tag{4}$$

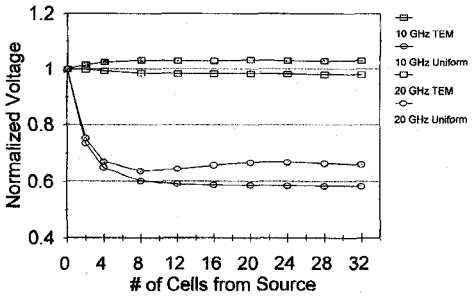


Fig. 3. Normalized voltage calculated at various points along the center conductor for a microstrip line for two different sources at the frequencies (a) 10 GHz and (b) 20 GHz. These graphs show that for the quasi-TEM source the fields converge closer to the source (i.e., in fewer number of cells) than when using a uniform source excitation.

where $x = i\Delta x$ and $z = k\Delta z$. With this method, improved convergence to actual field distributions occurs. To check the improvement gained by using this type of source, a uniform microstrip line was analyzed with parameters $\epsilon_r = 2.2$, $w/h = 3.0$, and $h = .6$ mm. The microstrip line was modeled using symmetry with $\Delta x = \Delta y = \Delta z = .15$ mm. The size of the FDTD grid used was $nx = 60$, $ny = 100$, and $nz = 40$. Fig. 3 shows the ratio between the steady-state voltage at various points along the microstrip line to the voltage at the source plane for two frequencies, 10 and 20 GHz. Convergence is defined to be when the steady-state voltage has changed negligibly between two voltage points. As can be seen from Fig. 3, the uniform source reaches convergence at a distance of about 20 cells from the source, whereas the source using the quasi-TEM template converges in approximately 4–8 cells. The 2-D quasi-TEM solution generally converged within 500 iterations taking less than 0.5 seconds of CPU time on an IBM RISC 6000 workstation. This extra expenditure is more than made up by the time and memory savings that come from the smaller FDTD lattice allowed by using the quasi-TEM source.

The time dependence of the source, $P(t)$ in (2), is chosen depending on the problem at hand. For applications where S-parameters or other frequency dependent data is required, a pulse is used such that its frequency content covers the desired frequency range. The highest frequency at which parameters should be extracted is generally limited by the size of the Yee cell in the FDTD grid. The frequency at which the smallest Yee-cell dimension is $\lambda/20$ is usually chosen as the highest frequency at which data can be accurately simulated. For the Gaussian pulse, $P(t)$ is given by

$$P(t) = \exp\left[\frac{(t-t_0)^2}{T^2}\right] \tag{5}$$

where t_0 governs the value of the pulse at turn on and T governs the width of the pulse in time. If T in (5) is expressed as $T = \sqrt{2.303A}/\pi f_0$, then the source spectrum will be $-A$ dB below the dc value at the frequency f_0. For this research, $A = 40$ is selected for $f_0 = 80$ GHz and t_0 is selected so that when the source is turned on and off, $P(t) = 10^{-20}$.

B. Absorbing Boundary Conditions

In order to minimize reflections at the lattice boundaries, accurate absorbing boundary conditions must be implemented. Various ABC's have been presented for use in planar geometries [8], [11], and [15]–[18]. For this paper, the absorbing boundary conditions of Zhang and Mei [8] were utilized at the two planes (ABCD) and (EFGH) and first order boundary conditions were utilized on the other lattice walls. Almost all of the boundary conditions employed in FDTD for analysis of planar guiding structures assume a constant velocity of light for electromagnetic waves incident on the boundaries. Most planar structures exhibit a frequency dependent velocity of propagation and pulse excitation sources contain a broad band of frequencies. Therefore no one value of velocity of light will satisfy the absorbing boundary conditions and the optimum value will be different at the various frequencies of the source spectra. An optimum value of the speed of light needs to be determined in order to minimize the reflected energy at the lattice boundaries and therefore obtain the most accurate results, preferably not by trial and error. For this paper, a weighted $\epsilon_{r,\text{eff}}$ is calculated in order to minnimize the reflections [16]. Fig. 4 shows the frequency spectrum of a typical Gaussian pulse along with $\epsilon_{r,\text{eff}}$. As can be seen, for the Gaussian pulse the lower frequencies contain more power and therfore the value chosen for $\epsilon_{r,\text{avg}}$ should be shifted more toward the lower frequency values. In order to accomplish this weighting, $\epsilon_{r,\text{avg}}$ is chosen as

$$\epsilon_{r,\text{avg}} = \frac{\int_0^{f_{\max}} |S(f)|^2 \epsilon_{r,\text{eff}}(f)\, df}{\int_0^{f_{\max}} |S(f)|^2\, df} \tag{6}$$

where $S(f)$ is the Fourier transform of the incident waveform on the boundary, $\epsilon_{r,\text{eff}}(f)$ is the frequency dependent effective dielectric constant and $f_{\max}$ is the maximum frequency at which the DFT is calculated. Equation (6) weights the value of $\epsilon_{r,\text{avg}}$ according to the energy of the source thereby minimzing the power reflected at the lattice boundaries. It should be noted that while a similar procedure was suggested earlier, it was not implemented in the presented results [16]. Fig. 5 shows the ratio of reflected energy to incident energy from the back lattice wall (plane EFGH) for various values of $\epsilon_{r,\text{eff}}$ for two different microstrip lines using two different ABC's. The normalized energy was calculated as

$$\text{Energy}_{\text{norm}} = \frac{\text{Energy}_{\text{ref}}}{\text{Energy}_{\text{inc}}} \tag{7}$$

where

$$\text{Energy}_{\text{inc}} = \sum_{t=0}^{t=M\Delta t} V^2 \tag{8}$$

and

$$\text{Energy}_{\text{ref}} = \sum_{t=(M+1)\Delta t}^{t=N\Delta t} V^2 \tag{9}$$

where M is a time step in the FDTD simulation and is chosen such that the incident pulse has traveled passed the observation point and the reflected energy has not yet returned and N is the last time step of the simulation. As can be seen from Fig. 5, the weighted average value of the effective dielectric constant yielded the least amount of reflected energy.

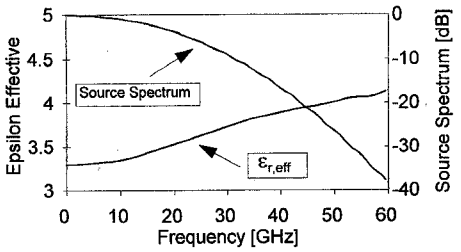


Fig. 4. Typical source spectrum of a Gaussian pulse and the effective dielectric constant of a microstrip line as a function of frequency.

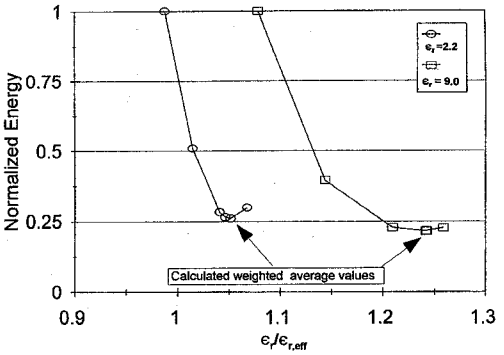


Fig. 5. Normalized energy reflected off of the end absorbing boundary in the FDTD lattice (Plane EFGH in Fig. 1) versus ϵ_r used for the boundary. To help plot results of two microstrip cases on the same figure, ϵ_r is normalized to low-frequency value of ϵ_{reff} which is calculated using available empirical formulas for microstrip lines. The first graph shows the calculated reflected energy for first order absorbing boundaries at the EFGH plane for a microstrip line of $\epsilon_r = 2.2$. In this case, the variable ϵ_r values on the horizontal axis were normalized to $\epsilon_{reff} = 1.87$ which was obtained from a low frequency empirical formula. In the other curve, the super absorbing boundary conditions of [8] were used at the EFGH plane and a microstrip of $\epsilon_r = 9.0$ was used. ϵ_{reff} from an empirical formula which was used to normalize the data in this case is $\epsilon_{reff} = 6.12$. In both cases, the calculated weighted $\epsilon_{reff,avg}$ yielded the minimum reflected energy.

III. Results

Before presenting typical FDTD results and the corresponding equivalent circuits, we validated our FDTD simulation by modeling a via structure reported in [19]. In this reference, both numerical and experimental results were reported and, hence, is expected to provide a good validation for our code. Fig. 6 shows the obtained FDTD results from our code and the experimental results reported in [19]. From these results, it may be seen that our FDTD code provides accurate data in a board frequency band except at the via resonant frequency, where some discrepancy in the values may be observed. This discrepancy may be either from the experimental measurements or the exact dimensions used in the FDTD simulation.

The first new FDTD data are related to the study of the effect of bond wires on electronic interconnects. The use of bond wires to connect an IC die to the leadframe (such as a DIP) is an area of concern in electronic packaging. While at low frequencies a bond wire is mostly inductive, at higher frequencies, a bond wire behaves as a high-impedance transmission line. Fig. 7 shows the schematic for analyzing the bond wire using conductor-backed coplanar waveguides with a Gallium–Arsenide substrate ($\epsilon_r = 13$). For this geometry,

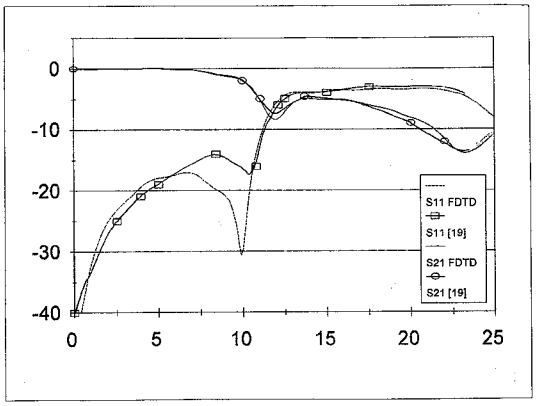


Fig. 6. Comparison of the FDTD results with a single via experimental data reported in [19]. The via was in a microstrip with $\epsilon_r = 3.4$, $W = 3.4$, $H = 1.6$ mm, $D_{\text{Pad}} = D_{\text{Thruhole}} = 3.9$ mm, $D_{\text{Via}} = 0.7$ mm and $D_{\text{Air}} = 0$ (a schematic illustrating the dimensions of a similar via is shown in Fig. 11).

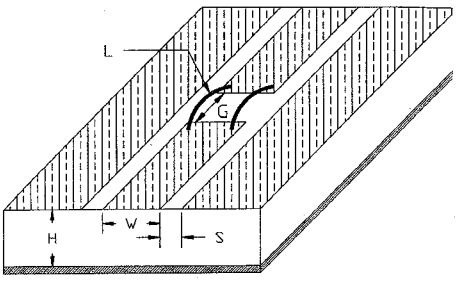


Fig. 7. Sketch of a coplanar waveguide with 1 mil bond wires. Dimensions are $W = 200\mu$m, $H = 850\mu$m, $S = 125\mu$m, L =1.2 mm, G =1 mm, $\epsilon_r = 13$. FDTD lattice: 80×200×100 ($n_x \times n_y \times n_z$) with $\Delta x = \Delta z = 25\mu$m and $\Delta y = 50\ \mu$m.

a single bond wire located at the center of the conductor was used. The FDTD variables were $\Delta x = \Delta z = .025$ mm and $\Delta y = .050$ mm. In order to help isolate the bond wire, only the center conductor had a bond wire, the ground lines were assumed uniform throughout. The bond wire was assumed to be a perfect conductor and one Yee cell thick, and had a total length of 2.2 mm. Fig. 8 shows the obtained S-parameters from the bond wire. An equivalent circuit for the structure was developed and the obtained equivalent circuit parameters are shown in Fig. 9. The S-parameters of the equivalent circuit are shown together with the FDTD results in Fig. 8 for comparison. The values were obtained using HP EESof's Libra [20] by optimizing the circuit and minimizing the difference between the S-parameters obtained from FDTD and those of the equivalent circuit. The series resistor-capacitor branch (R3-C4) helps to account for higher order effects such as radiation at higher frequencies. At lower frequencies, this branch can be neglected. The resistances R1 and R2 are for losses in the bond wire, but because the metal was assumed to be perfectly conducting these resistances are negligible. In order to reduce the inductive effects of the bond wire, it is common to use two bond wires in parallel. The same circuit model as for the single bond wire case was used to model the case of two parallel bond wires, and the results are shown in Fig. 10 with the component values shown in Fig. 9, Case B. As can be seen, the equivalent inductance was nearly halved by using two bond

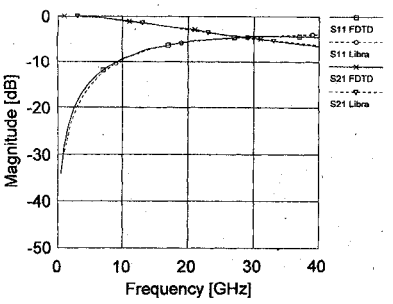
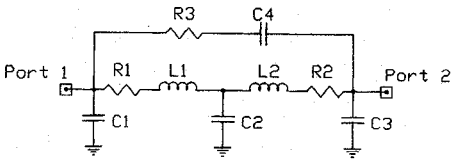


Fig. 8. S-parameters of the coplanar waveguide sketched in Fig. 7 using only one bond wire located in the middle of the center conductor. Results from both the FDTD code and the equivalent circuit model are included.



Component	Case A	Case B
R1 and R2	0	0
C1 and C3	0.0077 pF	0.0212 pF
L1 and L2	0.315 nH	0.188 nH
C2	0.0037 pF	0.009 pF
C4	0.120 pF	0.417 pF
R3	319.7 Ω	190.1 Ω

Fig. 9. Equivalent circuit for the single bond wire on the coplanar waveguide of Fig. 7. Case A shows the component values for the single bond wire case and Case B shows values for the case of two parallel bond wires.

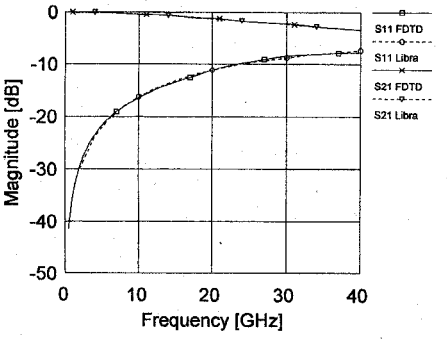


Fig. 10. S-parameters of the coplanar waveguide of Fig. 7 when using two bond wires in parallel. Results from both the FDTD code and the equivalent circuit model are shown for comparison.

wires. As a note, additional FDTD simulations showed that the best response (largest S_{21}) was obtained with the bond wires as close to the edges of the conductor as possible. This is as expected because it is at these locations where the current density is highest on the stripline.

Another practical example which we examined using the developed FDTD code is the high frequency performance of a via. Vias affect the high-frequency operation of a circuit by its discontinuity on a uniform transmission line [19], [21]. Fig. 11 shows the schematic of two vias in close proximity to one another. In order to isolate the vias, the microstrip

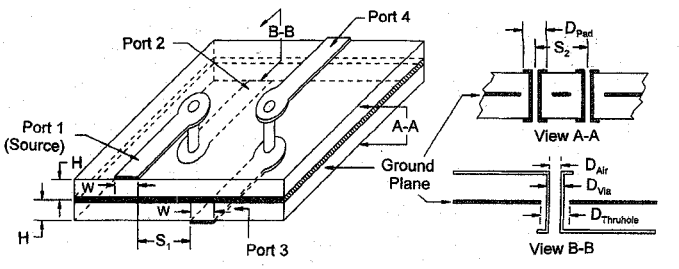


Fig. 11. Schematic diagram illustrating the geometry of two microstrip lines with vias. To emphasize the coupling between vias, the microstrip lines were placed on opposite sides of the ground plane. Dimensions are $W = 1.0$ mm, $H = 0.5$ mm, $S_1 = 0.6$ mm, $S_2 = 1.6$ mm, $\epsilon_r = 4.4 D_{\mathrm{Pad}} = 1.0$ mm and $D_{\mathrm{Thruhole}} = 1.6$mm, $D_{\mathrm{Via}} = 0.8$ mm and $D_{\mathrm{Air}} = 0.6$ mm. FDTD lattice: 140×200×96 with $\Delta x = \Delta y = \Delta z = 0.1$ mm.

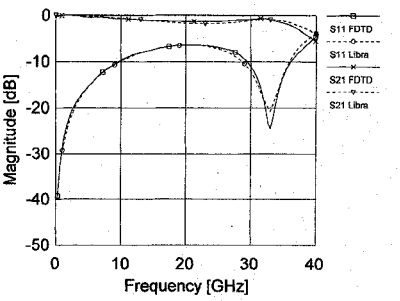


Fig. 12. S-parameters versus frequency of a microstrip line with a single via (Fig. 11). Results from both FDTD and the equivalent circuit analyzed with Libra are shown for comparison.

lines were placed on opposite sides of the ground plane. This way, the ground plane minimizes the coupling between the microstrip lines and hence the characteristics of the coupling between vias are emphasized. The vias are assumed to be air-filled cylinders similar to plated through holes found in multilayer printed circuit boards. The dielectric chosen was that of epoxy-glass printed circuit boards ($\epsilon_r = 4.4$). The results for a single via are shown in Fig. 12 along with the results from the obtained equivalent circuit model shown in Fig. 13. The via had dimensions of $D_{\mathrm{Thruhole}} = 1.6$ mm, $D_{\mathrm{pad}} = 1.0$ mm, $D_{\mathrm{Via}} = 0.8$ mm and $D_{\mathrm{air}} = 0.6$ mm. The same equivalent circuit was used as in the bond wire case due to the inductive nature of the via at lower frequencies. To help match the calculated FDTD and the equivalent circuit S-parameter results at the higher frequencies (>20 GHz), a second R-C branch was added to the equivalent circuit. As can be seen, with the addition of the second R-C branch, the equivalent circuit and FDTD results agree quite well. This same model was then used for the two via case, but mutual inductors were used to model the coupling between the two vias. The S-parameters obtained from FDTD and the equivalent circuit are shown in Fig. 14. Fig. 14(a) shows the results for S_{11} and S_{21} and Fig. 14(b) shows the results for S_{31} and S_{41}. Both FDTD and Libra simulation results are shown. The equivalent circuit is shown in Fig. 15. The equivalent circuit model shows good agreement at lower frequencies (up to 12 GHz), but continues to deviate beyond this frequency. This may be due to the fact that the equivalent circuit does not take into account higher order effects such as radiation and

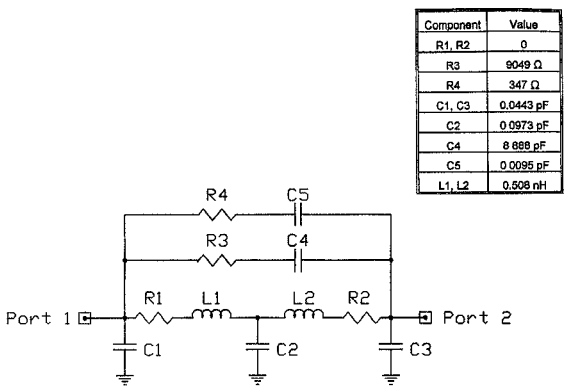
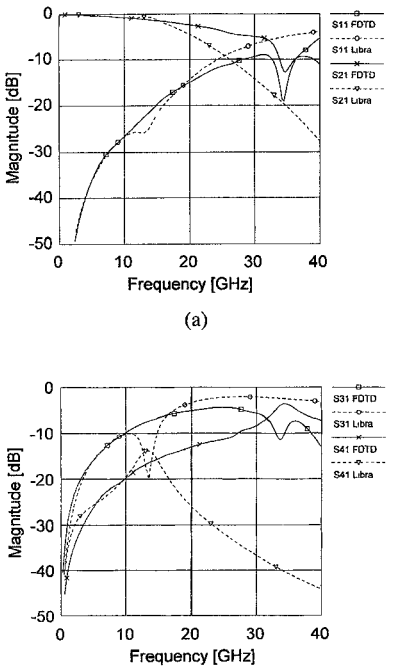


Fig. 13. Equivalent circuit of the single via geometry shown in Fig. 11.



(a)

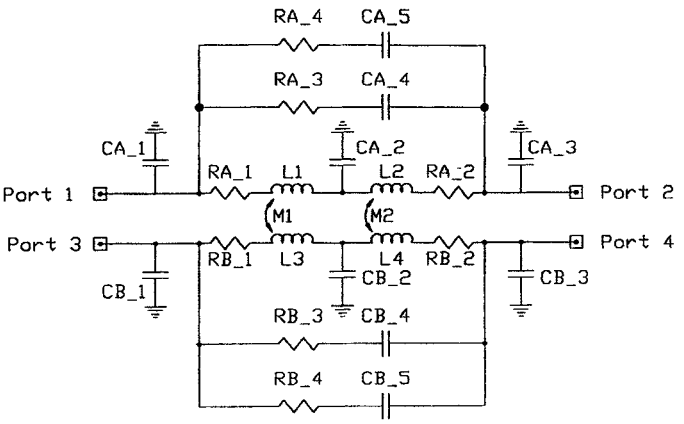
(b)

Fig. 14. *S*-parameters versus frequency of the two microstrip lines with vias shown in Fig. 11. Results from both FDTD and the equivalent circuit analyzed with Libra are shown for comparison. Dimensions are the same as those given in Fig. 11. Fig. 14(a) shows the reflection S_{11} and the transmission S_{21} results, while Fig. 14(b) shows the cross coupling between the vias S_{31} and S_{41} *S*-parameter data.

the resonance effects seen around 35 GHz. In order to account for the different coupling to all of the ports, different values of inductances and mutual inductances are clearly needed.

IV. Conclusion

An FDTD code was developed to analyze the high-performance characteristics of complex packaging structures. A method for determining the optimum value of a weighted $\epsilon_{r,\text{eff}}$ for use in the absorbing boundary conditions when pulse excitation is used in FDTD was presented and was shown to yield the value that minimizes reflections at the boundary walls. Also, a quasi-static TEM solution was used to launch the source in the lattice and was shown to reduce



Component	Via A	Via B
R1, R2	0	0
R3	6776	6314 Ω
R4	1251	1086 Ω
C1	0.063	0.071 pF
C2	0.24	0.74
C3	.019	1.49 pF
C4	9.69	9.50 pF
C5	99.8	104.9 pF
L1	0.168 nH	
L2	0.282 nH	
L3		0.508 nH
L4		0.311 nH
M1		0.289 nH
M2		0

Fig. 15. Equivalent circuit of the two microstrip lines with vias shown in Fig. 12.

the number of cells required before an established EM wave is produced and guided down the transmission line. Various packaging geometries were analyzed and equivalent circuits were developed, including one or more bond wires and both single and coupled vias. Results indicate that using multiple bond wires in parallel improve the high-frequency performance. Also, analysis of vias showed resonance effects that made the development of an equivalent circuit over a broad frequency band (up to 40 GHz) rather challenging. Equivalent circuits for frequencies up to 12 GHz were presented.

Future plans include the use of the developed FDTD code to further examine complex package structures including perforated ground planes, resonant effects of vias, crossovers, and radiation effects. Based on the frequency and time-domain results available from the developed FDTD code, we will also attempt to produce guidelines to predict time-domain performance of electronic packages from measured or calculated frequency-domain *S*-parameters. *S*-parameters seem to be common and well understood by the RF/Microwave engineer, while further efforts need to be focused in order to intuitively and/or empirically relate characteristics and

benchmarks of the S-parameters to the time-domain and digital performance of electronic packages.

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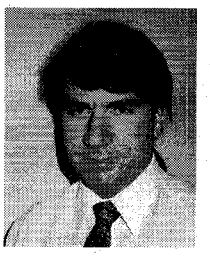

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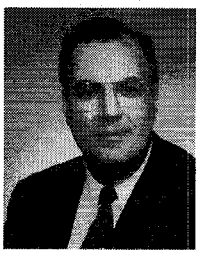

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